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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,332	08/02/2006	Juergen Schmidt	01012-1026	6695

30671 7590 01/15/2008
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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

MAIL DATE	DELIVERY MODE
01/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,332	SCHMIDT, JUERGEN	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/13/05 and 4/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, the phrase "whose frequency may be divided if required" renders the claim indefinite. The claim defines no objective standard for determining when division is required and thus one of ordinary skill in the art would not know how to ascertain when division is or is not required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asami (US 4,904,948).

With regard to claim 1, Asami discloses in Figs. 1-7 a circuit for a phase/frequency-locked loop comprising a phase/frequency comparator (as shown in Fig. 6) and a frequency-generating oscillator (6 in Fig. 1), the phase/frequency comparator having two edge-triggered

storage devices (1 and 2 in Fig. 6) which are respectively set by an edge of a reference-frequency signal (A) and by an edge of an output-frequency signal (B) from the phase/frequency locked loop, and which are each reset by an output signal (RS) from a resetting logic unit (NG2, NG4) to whose inputs are supplied the output signals from the two edge-triggered storage devices, wherein the output signal from the resetting logic unit is only activated (output a pulse with logic Lo) when both the output signals (OA, OB) from the two edge-triggered storage devices have been activated (at logic Hi), and is only de-activated (at logic Hi) when both the output signals from the two edge-triggered storage devices have been deactivated (at logic Lo; as depicted in Fig. 7), and the resetting logic unit is implemented by means of an asynchronous level-triggered RS storage device of inverse logic. Figs. 1-7 of Asami shows a circuit meeting all of the claimed limitations except for the resetting input of the asynchronous level-triggered RS storage device having the output signal from an NAND gate (NG3) supplied to it instead of the output signal from an NAND gate (NG3) supplied to it instead of the output signal from an OR gate (21 instant Fig. 4) supplied to it. However, it is notoriously well known in the art that an OR-function can be implemented both by an OR-gate with non-inverted signals and by an NAND-gate with inverted signals and that both circuit arrangements are mutually interchangeable, without any unexpected results in circuit operation. The optimal arrangement should be selected according to the conditions of the particular circuit environment. Therefore, it would have been obvious to one skilled in the art at the time of applicant's invention was made to replace the NAND-gate (NG3 of Asami) with an OR-gate for the expected advantage of reducing wiring overheads. Since, in a modified circuit arrangement with an OR-gate is used, the inverted outputs Oa and Ob of storage elements 1 and 2 are no longer necessary because the inputs of the

OR-gate would be connected to the outputs OA and OB of storage elements 1 and 2. Furthermore, the recitation "and in that the two edge-triggered storage devices each have only an output of non-inverted logic" is also met by the reference.

With regard to claim 2, wherein the output of the edge-triggered storage device (1), to whose input the reference-frequency signal (A) is applied is fed to the frequency-generating oscillator (6), and the output of the edge-triggered storage device (2), to whose input the output-frequency signal, whose frequency is divided by a FREQUENCY DIVIDER CIRCUIT 7), is applied is fed to the frequency-generating oscillator (6) to reduce the frequency of the output-frequency signal.

With regard to claim 3, wherein the signals (OA, OB) at the outputs of the two edge-triggered storage devices (1, 2) are connected to the frequency-generating oscillator (6) via an interposed loop filter (5) for stabilizing the phase-frequency-locked loop.

With regard to claim 5, the frequency of the output-frequency signal from the phase/frequency-locked loop is reduced by a factor M by means of a frequency divider (7), upstream of the input of the phase/frequency comparator.

Claim 6 is similarly rejected; note the above discussion with regard to claim 1.

5. Claim 4, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Asami as applied to claim 1 above, and further in view of Meyers et al. (US 6,771,096; herein after "Meyers").

The above discussed circuit of Asami meets all the claimed limitations except for a frequency divider (2 in instant Fig. 3) for dividing the frequency of the reference-frequency signal. Meyers teaches in Fig. 1 a circuit having a frequency divider (14) as recited in the claim.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that frequency divider, for dividing the frequency of the reference-frequency signal A, taught by Meyers in the circuit of Asami for the advantage of allowing the use of higher frequency reference sources.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Chou et al. (US 7,102,448) is cited as of interest because it discloses a phase frequency detector used in phase locked loop.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hai L. Nguyen
Patent Examiner
January 8, 2008